Tackling the Little Box Challenge - New circuit architectures to achieve a 216 W/in$^3$ power density 2 kW inverter

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Outline

- Competition background
  - Technical challenges

- Twice line frequency ripple compensation
  - Conventional approaches
  - Series-stacked buffer architecture
  - Experimental measurements

- AC waveform generation
  - Conventional approaches
  - Flying-capacitor multi-level converter background
  - Integrated switching cell development
  - Experimental results

- Performance evaluation and comparison

- Lessons learned and future research directions
Google/IEEE Little Box Challenge

- 2 kW, single-phase 240 V, 60 Hz AC
- Example usage: solar inverter, electric car charger, grid storage integration
- Current state-of-the-art: 95% efficiency, 400 in³.
- Target goal: >95% efficiency, 10x smaller (40 in³), must run for 100 hours
- $1M prize to winning entry
To Participate or not Participate?

- **Why not participate?**
  - We had no prior inverter experience
  - Winning solution likely one that sacrifices reliability (e.g., 101 hour operation)
  - Rules more suitable for industry
    - 1-year timeline to develop inverter from scratch
    - Rigorous testing protocol -> robustness required
    - FCC Class B (including radiated!)
  - Most people told us that Kolar’s team at ETH will likely win anyway

- **Why participate?**
  - Compete against the best teams in the world
  - Students will learn valuable skills
    - EMI, packaging, thermal, etc.
  - A chance to compare our new research ideas against a common benchmark
Our Goal

Develop a radically different solution – make significant research contribution to the field of power electronics. May not win competition, but will have long-term impact.
Chris Barth
- Integration
- Mechanical
- Thermal
- Capacitor evaluation

Yutian Lei
- Inverter design
- Inverter control

Shibin Qin
- Twice-line-frequency buffering
- System control

$30k funding through Google Academic Grant
Key Technical Challenges

\[ E_{store} = \frac{P_{dc}}{2\pi f_{line}} \]
Capacitor as energy storage

\[ E_{store} = \frac{P_{dc}}{2\pi f_{line}} = \frac{1}{2} C V_{\text{max}}^2 - \frac{1}{2} C V_{\text{min}}^2 \]
\[ = C \times \frac{1}{2} (V_{\text{max}} + V_{\text{min}}) \times (V_{\text{max}} - V_{\text{min}}) \]

\[ \Gamma_{EUR} = \frac{E_{\text{buf,peak}}}{E_c(V_{\text{max}})} = \frac{E_c(V_{\text{max}}) - E_c(V_{\text{min}})}{E_c(V_{\text{max}})} \]
Active Filtering – Ripple Port Converter

Advantages

- Capacitor ripple decoupled from bus ripple
- Increased energy utilization of capacitor
  - Smaller overall size

Disadvantages

- High buffer converter power rating
- High voltage stress
  - Low switching frequency, large inductor(s)
- Overall efficiency reduced:

\[ \eta_{\text{buf}} = \eta_{\text{dc-ac}} = 95\% \]
\[ \eta_{\text{total}} = 92.4\% \]

Krein et al., Minimum energy and capacitor requirement for single-phase inverters and rectifiers using a ripple port, IEEE TPELS, Nov, 2012
Hu et al., A single-stage micro-inverter without using electrolytic capacitors, IEEE TPELS, June, 2013
Stacked Switched-Capacitor Buffer

Advantages

- No inductor
- Potentially higher efficiency (slow switching action)
- Reduced switch rating possible

Disadvantages

- Large bus ripple
- Lower energy utilization of capacitors
- Increased circuit complexity
  - Gate drivers, etc.

Series-Stacked Buffer Architecture
A series-connected buffer converter

- Reduced voltage stress ($C_1$ blocks majority of voltage)
  - Enable low voltage transistors - > Buffer converter size reduction
- Partial power processing (extreme efficiencies possible)
- Low power rating of buffer converter
  - Size reduction

Qin et al., A High-Efficiency High Energy Density Buffer Architecture for Power Pulsation Decoupling in Grid-Interfaced Converters, ECCE 2015
Circuit Architecture - Overview

- $i_{buf}$ controlled to provide difference between $i_s$ and $i_{inv}$
- $v_{c1} + v_{ab}$ constant
- Buffer converter processes fraction (7% here) of overall power -> greatly improved efficiency
Control Challenge: Voltage Balancing

- Buffer converter introduces loss
  - $C_2$ will slowly discharge, unless compensated
  - Must provide additional charge to $C_2$
- Can “recharge” $C_2$ through external means - undesirable
Buffer converter power

\[ i_{\text{buf}} \times v_{ab} = i_{\text{buf}} \times (v_{\text{bus}} - v_{C1}) \]

\[ i_{\text{buf}} \rightarrow \text{pure AC}, v_{C1} \rightarrow \text{pure AC} \]

\[ v_{\text{bus}} \rightarrow \text{DC + small AC (ripple)} \]

Qin et al., Architecture and control of an high energy density buffer for power pulsation decoupling in grid-interfaced applications, COMPEL 2015 [Best paper award]
Hardware Implementation – Capacitor Choices

- **Metal film**
  - Very low loss
  - Constant capacitance
  - Low energy density

- **Ceramic**
  - Low loss
  - Capacitance reduced with applied voltage
  - High energy density

- **Electrolytic**
  - High loss
  - High constant capacitance
  - RMS current limited
  - Poor reliability
Experimental test setup is configured to measure energy storage over wide voltage swing.
- Voltage swing and bias are independently adjustable.
Experimental Results

- Experimental waveforms:
  - Film capacitor with constant capacitance
  - Ceramic capacitor with varying capacitance
Experimental Results

- Measured energy density for a range of capacitors and voltage ratings.

\[
Density = \frac{\text{Energy transferred per cycle (J)}}{\text{Capacitor volume (mm}^3\text{)}}
\]

Experimental Results

- Quality factor normalizes energy stored by loss.

$$Q = \frac{2\pi \times \text{energy stored}}{\text{energy dissipated per cycle}}$$
Hardware Prototypes

410 W/inch\(^3\)

~180 W/inch\(^3\)
Hardware Prototype – Energy Density

Design requirement:
- 2 kVA (PF = 0.7~1)
- 400 V ~ 450V bus voltage,
- 10 A peak to peak current

<table>
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<tr>
<th>Way of measurement</th>
<th>Volume</th>
<th>Power density</th>
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<tr>
<td>Rectangular box</td>
<td>4.88 inch^3</td>
<td>410 W/inch^3</td>
</tr>
<tr>
<td>passive component</td>
<td>2.01 inch^3</td>
<td>995 W/inch^3</td>
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</table>

99% efficiency across load range
Final Hardware Prototype

- EPC 2016C / LMG 5200 100 V switch
- TDK X6S capacitors
- TI Delfino F28377D

- Isolator ADuM5210
- Current sensing: LT1999
- Voltage sensing: LT1990
Experiment - Steady State Operation
Experiment - Transient Operation

25% load to 50% load

100% load to 75% load
Experiment - Efficiency

- Digital power meter, integral function to ensure accuracy
  - Same setup that was used to characterize capacitors
- Efficiency measurement excludes about 3 W control and gate driving power
Key Technical Challenges

\[ E_{\text{store}} = \frac{P_{\text{dc}}}{2\pi f_{\text{line}}} \]
Inverter – Conventional Topology

- Conventional Inverter
  - H-bridge (likely dual interleaved)
  - 650 V GaN transistors
  - High switch stress
  - High $dv/dt$
  - Large inductor
  - Localized hot spots
Multi-Level Flying-Capacitor Converter

- Inductor ripple frequency: $f_{sw} \times (N - 1)$
- Reduced ripple voltage amplitude: $V_{DC}/(N - 1)$
- Reduced switch voltage stress: $V_{DC}/(N - 1)$
- Heat spreading

T. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” PESC ’92
Multi-level Operation

\[ V_{in} \]

\[
\begin{array}{cccccccc}
S_{3a} & S_{2a} & S_{1a} & C_2 & C_1 & V_{sw} & V_{sw} \\
\hline
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & + & V_{in} - \frac{2}{3}V_{in} & \frac{1}{3}V_{in} \\
0 & 1 & 0 & - & + & \frac{2}{3}V_{in} - \frac{1}{3}V_{in} & \frac{1}{3}V_{in} \\
0 & 0 & 1 & - & + & \frac{1}{3}V_{in} & \frac{1}{3}V_{in} \\
1 & 1 & 0 & + & V_{in} - \frac{1}{3}V_{in} & \frac{2}{3}V_{in} \\
0 & 1 & 1 & - & + & \frac{2}{3}V_{in} & \frac{2}{3}V_{in} \\
1 & 0 & 1 & + & + & V_{in} - \frac{2}{3}V_{in} + \frac{1}{3}V_{in} & \frac{2}{3}V_{in} \\
1 & 1 & 1 & V_{in} & V_{in} \\
\end{array}
\]
Multi-level Operation

\[
\begin{align*}
S_{3a} & \quad S_{2a} & \quad S_{1a} & \quad C_2 & \quad C_1 & \quad V_{sw} & \quad V_{sw} \\
0 & \quad 0 & \quad 0 & \quad 0 & \quad 0 & \quad 0 \\
1 & \quad 0 & \quad 0 & \quad + & \quad V_{in} - \frac{2}{3}V_{in} & \quad \frac{1}{3}V_{in} \\
0 & \quad 1 & \quad 0 & \quad - & \quad + & \quad \frac{2}{3}V_{in} - \frac{1}{3}V_{in} & \quad \frac{1}{3}V_{in} \\
0 & \quad 0 & \quad 1 & \quad - & \quad - & \quad \frac{1}{3}V_{in} & \quad \frac{1}{3}V_{in} \\
1 & \quad 1 & \quad 0 & \quad + & \quad V_{in} - \frac{1}{3}V_{in} & \quad \frac{2}{3}V_{in} \\
0 & \quad 1 & \quad 1 & \quad - & \quad - & \quad \frac{2}{3}V_{in} & \quad \frac{2}{3}V_{in} \\
1 & \quad 0 & \quad 1 & \quad + & \quad - & \quad V_{in} - \frac{2}{3}V_{in} + \frac{1}{3}V_{in} & \quad \frac{2}{3}V_{in} \\
1 & \quad 1 & \quad 1 & \quad V_{in} & \quad V_{in}
\end{align*}
\]
**Multi-level Operation**

![Multi-level Operation Circuit Diagram]

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Multi-level Operation

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\text{Table:}\quad & S_3a & S_2a & S_1a & C_2 & C_1 & V_{sw} & V_{sw} \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & + & V_{in} - \frac{2}{3} V_{in} & \frac{1}{3} V_{in} \\
0 & 1 & 0 & 0 & \text{--} & \text{--} & \text{--} \\
0 & 0 & 1 & - & \text{--} & \frac{1}{3} V_{in} & \frac{1}{3} V_{in} \\
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Multi-level Operation

\[ V_{\text{in}} \]

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### Multi-level Operation

**Diagram:**

A circuit diagram showing the connection of various switches and capacitors, labeled with voltages and currents.

**Table:**

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\[ V_{sw} = \frac{1}{3}V_{in} \]
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<tbody>
<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>0</td>
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<td>+</td>
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<td>$V_{in} - \frac{2}{3}V_{in}$</td>
<td>$\frac{1}{3}V_{in}$</td>
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<tr>
<td>0</td>
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<td>+</td>
<td>$\frac{2}{3}V_{in} - \frac{1}{3}V_{in}$</td>
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</tr>
<tr>
<td>0</td>
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<td>-</td>
<td>$\frac{1}{3}V_{in}$</td>
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</tbody>
</table>
Multi-level Operation

<table>
<thead>
<tr>
<th>$S_{3a}$</th>
<th>$S_{2a}$</th>
<th>$S_{1a}$</th>
<th>$C_2$</th>
<th>$C_1$</th>
<th>$V_{sw}$</th>
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$V_{sw}$
Multi-level Operation

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</tr>
</tbody>
</table>

The diagram shows the operation of a multi-level converter with switching states and their corresponding voltages.
Multi-level Operation

<table>
<thead>
<tr>
<th>S_{3a}</th>
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<th>S_{1a}</th>
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<th>C_1</th>
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<td>-</td>
<td>\frac{1}{3}V_{in}</td>
<td>\frac{1}{3}V_{in}</td>
</tr>
</tbody>
</table>
Multi-level Operation

3 pulses in each switching period

1 pulse in each period
Our Proposed DC-AC Conversion Stage

Advantages

- Low voltage switch: $V_{DC}/(N-1)$, 450 V -> 75 V
- Alternates capacitor charging and discharging at switching frequency (compare to line frequency of MMC)
- Reduction in output filter size

T. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” PESC ’92
Implementation Challenges

Challenges

- Capacitor voltage balancing
  - Approach: natural balancing with phase-shifted PWM

- Gate driving complexity
  - Approach: Half-bridge gate drivers (LM5113) and integrated isolated dc-dc converter (ADUM5210)

- Parasitic inductance
  - Fast turn-on needed to reduce the V-I overlap loss during switching
  - High dv/dt causes $V_{ds}$ ringing

Few experimentally demonstrated examples of > 5 level flying capacitor multi-level inverter, and none switching in the 100’s of kHz at kW levels.
Implementation Challenges
Parasitic Loop Inductance
Integrated Switching Cell
Digital Control

- Control objective:
  - Generate correct amplitude
  - Switch only minimum inductance loops
  - Maintain capacitor voltage balance
Prototype #1

- 80 W/in$^3$, 98% efficient
- 2000+ total entries
  - July 23, 2015, 100+ submitted final report
  - 18 finalists selected to October 21, 2015 NREL testing
Growing the Team
Shrinking the Hardware
2 kW Hardware Prototype

Experimental Results

- **Output Voltage**
- **Output Current**
- **$V_{SW}$**

0.3% THD

- Measured EMI (dBuV)
- FCC Class B Limit

- Efficiency (%)
- Buffer Efficiency
- Inverter Efficiency
- Overall Efficiency
- Overall Efficiency including control and fans

- Output power (kW)
  - 0
  - 0.5
  - 1
  - 1.5
  - 2

- Measured
- FCC Class B Limit

- Frequency (Hz)
  - $10^5$
  - $10^6$
  - $10^7$
Resulting Performance

- 97.6% efficiency
- 216 W/in$^3$
- Commercial off-the-shelf components
- No electrolytic buffer capacitors
- All student-team
  - $30k$ budget (not including night and weekend work!)
- Innovation in both inverter and buffer converter
- Our 2$^{nd}$ iteration
  - Plenty of room for improvements
NREL Testing

- October 21\textsuperscript{st}, 2015 @ NREL
- Finalist symposium
  - 18 teams invited (3 no-shows)
- Drop-off inverters for extensive testing
  - Check all specifications
    - Ripple, EMI, temperature, etc
  - Load steps (extent unknown to teams)
  - 100 hour continuous operation
Performance Comparison (Best Estimate)

Excellent technical details/comparison by Prof. Johann Kolar at CIPS 2016 Keynote:
Difficult to exactly replicate testing scenarios
Research Impact

- Demonstrated the feasibility of multi-level flying capacitor power converters
  - At kW-scale
  - Using GaN technology
  - With 720 kHz effective switching frequency
- Achieved high efficiency and high power density through a new series-stacked active buffer
- Much work remains to be done for industry adoption
  - Gate driver, isolated power supplies, level shifting
  - Robustness, integration
- Approach likely to be relevant in applications where power density is a key requirement

Laid the foundation for several promising future research areas
Lessons Learned

- **Teams:**
  - Tempting to try to squeeze in too much innovation
  - Timeline very challenging
  - Great opportunity to learn from other teams
    - Fantastic technical discussions
    - Common “bonding experience”
  - Reliability was overlooked by many teams

- **Organizers:**
  - Difficult to set specs correctly the first time
  - Many good teams left out from finalist selection
  - Should consider allowing participants to test inverter at testing location

- **IEEE:**
  - Significant value in having a common benchmark to compare approaches
Acknowledgments

- Google
- Texas Instruments
- NASA
- TDK
- Grainger CEME at UIUC
The Team

Questions?
Estimated Power Loss Breakdown

- Active energy buffer (29%)
- Cooling fans (11%)
- Control (9%)
- Unfolder conduction (12%)
- Input switch (2%)
- FCMC Inductor (5%)
- EMC filter (5%)
- FCMC switching (15%)
- FCMC conduction (6%)
- Other (6%)
## Full Specifications

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Required</th>
<th>Achieved</th>
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</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>2 kVA</td>
<td>2 kVA</td>
</tr>
<tr>
<td>Volume</td>
<td>40 in³</td>
<td>9.52 in³ (152 cm³)</td>
</tr>
<tr>
<td>Power density</td>
<td>50 W/in³</td>
<td>216 W/in³ (13.2 W/cm³)</td>
</tr>
<tr>
<td>Rated input voltage</td>
<td>450 V</td>
<td>450 V</td>
</tr>
<tr>
<td>Rated output voltage</td>
<td>240 V&lt;sub&gt;RMS&lt;/sub&gt;</td>
<td>240 V&lt;sub&gt;RMS&lt;/sub&gt;</td>
</tr>
<tr>
<td>Efficiency (CEC Method)</td>
<td>95.0%</td>
<td>97.0%</td>
</tr>
<tr>
<td>Efficiency at rated power</td>
<td>95%</td>
<td>97.4%</td>
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<tr>
<td>Load power factor</td>
<td>0.7 – 1.0</td>
<td>0.7 – 1.0</td>
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<tr>
<td>Voltage THD</td>
<td>5%</td>
<td>0.3%</td>
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<tr>
<td>Input current ripple</td>
<td>20%</td>
<td>15%</td>
</tr>
<tr>
<td>Max. case temperature</td>
<td>60 ºC</td>
<td>57 ºC</td>
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<tr>
<td>EMC</td>
<td>FCC Class B</td>
<td>FCC Class B</td>
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</tbody>
</table>